

Description

DUAL DAMASCENE WIRING AND METHOD

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to the field of integrated circuits; more specifically, it relates to a dual damascene wiring structure and method of fabricating the dual damascene wiring structure.

[0003] BACKGROUND OF THE INVENTION

[0004] Dual damascene wiring, is used as a method of interconnecting semiconductor and other structures into integrated circuits because of the increased density over older interconnection methods. The industry is constantly looking for new dual damascene wiring structures that improve dual damascene wire fabrication and dual damascene wiring efficiency.

SUMMARY OF INVENTION

[0005] A first aspect of the present invention is a dual damascene structure, comprising: a first interconnect level comprising a first dielectric layer and including a multiplicity of first damascene or dual damascene conductive wires, each first damascene or dual damascene conductive wire extending from a top surface of the first dielectric layer a distance toward a bottom surface of the first dielectric layer, the distance less than, equal to greater than a thickness of the first dielectric layer; a second interconnect level directly above and in contact with the first dielectric layer, the second interconnect level comprising a second dielectric layer and including a multiplicity of second dual damascene conductive wires, each second dual damascene conductive wire extending from a top surface of the second dielectric layer a distance toward a bottom surface of the second dielectric layer, the distance less than a thickness of the second dielectric layer; and a dual damascene conductive via bar within the second interconnect level and integral with and extending from a bottom surface of one of the multiplicity of the second dual damascene conductive wires and a top surface of one of the multiplicity of the first dual damascene conductive wires, the dual damascene conductive via bar having a length

greater than its width, the length and width of the dual damascene conductive via bar extending in the plane defined by the top surface of the second dielectric layer.

[0006] A second aspect of the present invention is a method of fabricating a dual damascene method, comprising: forming a first interconnect level comprising a first dielectric layer and including a multiplicity of first damascene or dual damascene conductive wires, each first damascene or dual damascene conductive wire extending from a top surface of the first dielectric layer a distance toward a bottom surface of the first dielectric layer, the distance less than a thickness of the first dielectric layer; forming a second interconnect level directly above and in contact with the first dielectric layer, the second interconnect level comprising a second dielectric layer and including a multiplicity of second dual damascene conductive wires, each second dual damascene conductive wire extending from a top surface of the second dielectric layer a distance toward a bottom surface of the second dielectric layer, the distance less than a thickness of the second dielectric layer; and forming a dual damascene conductive via bar within the second interconnect level and integral with and extending from a bottom surface of one of the multiplicity

of the second dual damascene conductive wires and a top surface of one of the multiplicity of the first dual damascene conductive wires, the dual damascene conductive via bar having a length greater than its width, the length and width of the dual damascene conductive via bar extending in the plane defined by the top surface of the second dielectric layer.

[0007] A third aspect of the present invention is a method of fabricating a dual damascene structure, comprising: (a) providing a substrate; (b) forming a dielectric layer on the top surface of the dielectric layer; (c) forming a via bar opening in the dielectric layer, the via bar opening having a length greater than its width, the length and width of the via bar opening extending in the plane defined by the top surface of and dielectric layer, the via bar opening extending through the entire thickness of the dielectric layer; (d) etching a first trench in the dielectric layer, the first trench aligned to the via bar opening, the first trench extending from the top surface of the dielectric layer toward a bottom surface of the dielectric layer a distance less than a thickness of the dielectric layer; (e) applying an anti-reflective coating to a top surface of the dielectric layer, the antireflective coating filling the via bar opening;

(f) applying a masking layer to a top surface of the anti-reflective coating; (g) etching the antireflective coating from the via bar opening and forming a first trench in the dielectric layer over the via bar opening, the first trench extending from the top surface of the dielectric layer toward the bottom surface of the dielectric layer a distance less than a thickness of the dielectric layer; (h) removing the masking layer and any remaining antireflective coating; and (i) filling the first trench and the via bar opening with a conductor.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0009] FIGs. 1A through 1F are cross-sectional views illustrating fabrication of the damascene wiring elements is according to the present invention;

[0010] FIG. 2 is a top plan view of FIG. 1F;

[0011] FIG. 3A is a top view and FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A illustrating various combi-

nations of dual damascene wires and dual damascene via bars according to the present invention;

[0012] FIG. 4A is a plan view and FIG. 4B is a cross-sectional view through line 4B-4B of FIG. 4A illustrating an inductor according to the present invention; and

[0013] FIG. 5A is a plan view and FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A illustrating a capacitor according to the present invention.

DETAILED DESCRIPTION

[0014] A damascene process is one in which wire trench or via openings are formed in a dielectric layer, an electrical conductor deposited on a top surface of the dielectric of sufficient thickness to fill the trenches and a chemical-mechanical-polish (CMP) process performed to remove excess conductor and make the surface of the conductor co-planer with the surface of the dielectric layer to form a damascene wires (or damascene vias).

[0015] A dual damascene process is one in which via openings are formed through the entire thickness of a dielectric layer followed by formation of trenches part of the way through the dielectric layer in any given cross-sectional view. All via openings are intersected by integral wire trenches above and by a wire trench below, but not all

trenches need intersect a via opening. An electrical conductor is deposited on a top surface of the dielectric of sufficient thickness to fill the trenches and via opening and a CMP process performed to make the surface of the conductor in the trench co-planar with the surface the dielectric layer to form dual damascene wire and dual damascene wires having integral dual damascene vias.

[0016] FIGs. 1A through 1F are cross-sectional views illustrating fabrication of the damascene wiring elements is according to the present invention. In FIG. 1A, formed on a top surface 100 of a substrate 105 is a dielectric diffusion barrier layer 115. Formed on a top surface 110 of dielectric diffusion barrier layer 115 is an interlevel dielectric (ILD) layer 120. ILD layer 120 may include additional layers of interlevel dielectrics and dielectric diffusion barrier layers.

Substrate 105 may include integrated circuit devices such as field effect transistors (FETs), bipolar transistors including SiGe bipolar transistors, diodes, resistors, capacitors and/or inductors as well as contacts to these devices connecting them to wiring structures that will be formed in dielectric diffusion barrier layer 115 and ILD layer 120.

[0017] Examples of dielectric diffusion barrier layer 115 materials include, but are not limited to silicon nitride and silicon

carbide and other dielectric materials. In ILD layer 120, examples of ILD may include, bulk or porous silicon oxide, $\text{SiC}_x\text{O}_y\text{H}_z$, SiLK^{TM} (poly(arylene) ether) manufactured by Dow Chemical, Midland, MI, and other dielectric materials. In one example, dielectric diffusion barrier layer 115 is SiCN or Si_3N_4 and is about 50 nm to about 10 mm thick and ILD layer 120 is about 200 nm to about 6 microns thick.

[0018] In FIG. 1B, a photoresist layer 125 is formed on a top surface 130 of ILD layer 120 and openings 135A, 135C, 135D and 135E are formed in the photoresist layer in respective regions 140A, 140C, 140D and 140E by removal of the photoresist layer in these regions. Openings 135A, 135C, 135D and 135E may be formed by any of a number of photolithographic processes well known in the art. If a bottom anti-reflective coating (BARC) is not then top surface 130 of ILD layer 130 is exposed in openings 135A, 135C, 135D and 135E. Alternatively, a BARC deposited using spin on or chemical vapor deposition (CVD) methods as known in the could be employed over top surface 130 of ILD layer 120 and under photoresist layer 125. Photoresist layer 125 is not removed in a region 140B.

[0019] In FIG. 1C, via opening 145A, and via bar openings 145C,

145D and 145E have been formed in respective region 140A, 140C, 140D and 140E of ILD layer 120 wherever the ILD layer is not covered by photoresist layer 125 using, for example, a reactive ion etch (RIE) process selective to ILD layer 120 over dielectric diffusion barrier layer 115. Any number of suitable RIE processes that are well known in the art may be used. An etch process is to selective to a first layer over a second layer when the first layer etches at a faster rate than the second layer. Top surface 110 of dielectric diffusion barrier layer 115 is exposed in via opening 145A and via bar openings 145C, 145D and 145E. Via opening 145A has a width W1, via bar opening 145C has a width W2, via bar opening 145D has a width W3 and via bar opening 145E has a width W4. In a first example, $W1=W2=W3=W4$. In a second example, W1, W2, W3, and W4 are each about 140 nm. In a third example W2, W3 and W4 are each independently greater than W1.

[0020] In FIG. 1D, photo resist layer 125 (see FIG. 1C) is removed. An anti-reflective coating (ARC) 150 is applied to top surface 130 of ILD layer 120 filling via opening 145A and via bar openings 145C, 145D and 145E, as known in the art. A photoresist layer 155 is applied to a top surface 160 of ARC 150 and openings 165A, 165B, 165C and 165E are

formed in the photoresist layer in respective regions 140A, 140B, 140C and 140E. Openings 165A, 165B, 165C and 165E aligned to via or via bar openings in ILD layer 120 or to prior layer structures on the substrate as known in the art. Openings 165A and 165C are aligned respectively to via openings 145A and 145C in ILD layer 120 and are wider than trenches 145A and 145B. In one example ARC 150 is about 50 nm to about 800 nm thick in areas without via or via bar openings and fills the via and via bar openings void free in areas with via or via bar openings.

[0021] The presence of both via holes and via bars makes it more difficult to achieve good ARC layer 150 fill. Because the via bars have much higher volume than via holes, ARC layer 150 tends to be pulled down into the via bar, which results in increased sensitivity to etching through ARC layer 150 into or beyond dielectric layer 115 during the subsequent trough etch step. To avoid this, the fill of ARC layer 150 may need to be optimized, by increasing the shot size as part of the spin-apply process (e.g. for a 200mm wafer using Shipley AR14 ARC, increase the shot size from 1.5ml to 5ml); using multi step post ARC apply bakes to enhance the reflow into the via bars; or using a two step ARC apply and cure process, where the ARC is

applied and annealed twice. When the ARC fill is optimized, it is important to keep its thickness in areas without via holes or via bars minimized (e.g. 50–200nm) so that the trough etch process does not need to etch through excessive ARC with resulting degradation of the trench resist profiles.

[0022] In FIG. 1E, a sequential RIE process is performed to remove any ARC 150, ILD layer 120 and dielectric diffusion barrier layer 115 not protected by photoresist layer 155 (see FIG. 1D). Any number of suitable RIE processes that are well known in the art may be used. Photoresist layer 155 (see FIG. 1D) was removed as part of the etching, prior to etching diffusion barrier layer 115. In region 140A, a wire trench 170A having a depth D into ILD layer 120 and aligned over via opening 145A is formed. In region 140B, a wire trench 170B having the depth D into ILD layer 120 in region is formed. In region 140C, a wire trench 170C having the depth D into ILD layer 120 and aligned over via bar opening 145C is formed. In one example D is about 30 % to about 70 % of the thickness of ILD layer 120. Further dielectric diffusion barrier layer 115 is removed from the bottom of via opening 145A and via bar openings 145C and 145E. Wire trench 170A has a

width W5, wire trench 170B has a width W6 and wire trench 140C has a width W7. In a first example $W5 = W6 = W7$. In a second example W5 is greater than W1. In a third example W7 is greater than W2. In a fourth example W5, W6 and W7 are between about 140 nm and about 1mm.

[0023] FIG. 1F is a cross sectional view through line 1F–1F of FIG. 2. In FIG. 1F, in region 140A, a dual damascene wire 175A having an integral dual damascene via 180A is formed in wire trench and via 170A and opening 145A (see FIG. 1E). In region 140B, a dual damascene wire 175B is formed in wire trench 170B (see FIG. 1E). In region 140C, a dual damascene wire 175C having an integral dual damascene via bar 180C is formed in wire trench 170C and via bar opening 145D (see FIG. 1E). In region 140D, a dual damascene via bar 180D is formed in via bar opening 145D (see FIG. 1E). In region 140E, a dual damascene via bar 180E is formed in via bar opening 145E (see FIG. 1E). Dual damascene wires 175A, 175B and 175C, dual damascene via 180A, dual damascene via bars 180C, 180D and 180E each include an optional conductive liner 185 and a core conductor 190. Dual damascene wires 175A, 175B and 175C, dual damascene via 180A and dual damascene via

bars 180C, 180D and 180E and have been formed by a one or more depositions of a conformal conductive material to form conductive liner 185, deposition of a conductive seed layer (in one example, the conductive seed layer is copper), electro-plating or combinations thereof of a conductive material to form core conductor 190 followed by a CMP to remove all excess liner and core material from top surface 130 of ILD layer 120. Alternatively, the seed layer may be formed by a CVD process instead of an electroplating process. Examples of deposition processes include but is not limited to physical vapor deposition (PVD), ionized PVD (IPVD), self ionized plasma (SIP) deposition, hollow cathode magnetron (HCD) deposition, chemical vapor deposition (CVD) and atomic layer deposition (ALD).

[0024] The presence of both via holes and via bars makes it more difficult to achieve void free Cu fill. Because the via bars have much higher volume than via holes, and can be wider due either to design or process issues, care must be taken to avoid voids in the electroplated Cu. In particular, Cu electroplating is commonly performed in a three step process: 1) low current plating initiation step; 2) medium current plating gap fill step; 3) high current plating overbur-

den step. Step 3), the high current plating overburden step, has poor gap fill, and the medium current plating step 2) must be performed for enough time to completely fill the via bars.

[0025] Top surfaces 195A, 195B, 195C, 195D and 195E of respective dual damascene wires 175A, 175B and 175C and dual damascene via bars 180D and 180E are substantially co-planar with top surface 130 of ILD layer 120. One difference between dual damascene via bar 180D and dual damascene via bar 180E is dual damascene via bar 180D does not extend through dielectric diffusion barrier layer 115 while dual damascene via bar 180E does extend through dielectric diffusion barrier layer 115. One difference between dual damascene via bar 180C and dual damascene via bar 180E is dual damascene via bar 180C does not extend to top surface 130 of ILD layer 120) while dual damascene via bar 180E does extend to top surface 130 of ILD layer 120. (In a first sense dual damascene via bar 180C only extends to the bottom of dual damascene wire 175C, however since dual damascene via bar 180C is integral with dual damascene wire 175C, in a second sense dual damascene via bar 180C does extend to the top surface 130 of ILD layer 120. It is the first in the first

sense the comparison between dual damascene via bar 180C and dual damascene via bar 180E is made.)

[0026] The material of conductive liner 185 may be chosen to be a diffusion barrier to the material of core conductor 190. The material of dielectric diffusion barrier layer 115 may be selected to be a dielectric diffusion barrier to the material of core conductor 190. Suitable materials for conductive liner 185 include, but are not limited to tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride and combinations thereof. Suitable materials for core conductor 190 include, but are not limited to copper, tungsten, aluminum, aluminum-copper alloy and polysilicon.

[0027] FIG. 2 is a top plan view of FIG. 1F. In FIG. 2, dual damascene wire 175A extends in a lengthwise direction parallel to an L-axis and extends in a widthwise direction parallel to a W-axis orthogonal to the L axis the distance W5. Dual damascene via 180A extends in the L-axis direction a distance L1 and extends in the W-axis direction the distance W1. In one example, $L1=W1$. Dual damascene wire 175B extends in the L-axis direction an arbitrary distance and extends in the W-axis direction the distance W3. Dual

damascene wire 175C extends in the L-axis direction an arbitrary distance and extends in the W-axis direction the distance W7 and dual damascene via bar 180C extends the L-axis direction an arbitrary distance and extends in the W-axis direction the distance W2. Dual damascene via bar 180D extends in the L-axis direction an arbitrary distance and extends in the W-axis direction the distance W3. Dual damascene via bar 180E extends in the L-axis direction an arbitrary distance and extends in the W-axis direction the distance W4.

[0028] Dual damascene wire 175A and integral dual damascene via 180A is an example of a first wiring structure. Dual damascene wire 175B is an example of a second wiring structure. Dual damascene wire 175C and integral dual damascene via bar 180C is an example of a third wiring structure. Dual damascene via bar 180D is an example of a fourth wiring structure and dual damascene via bar 180E is an example of a fifth wiring structure of the present invention. As will be described infra, all five of these wiring structures along with others, such as terminal pads (which may be considered a type of wire) may be connected to each other and to devices such as (FETs), bipolar transistors including SiGe bipolar transistors, diodes, resistors,

capacitors and/or inductors to form integrated circuits.

[0029] In typical applications, several interconnect levels (each including dual damascene wires, dual damascene vias and dual damascene via bars formed in an ILD and optionally including a dielectric diffusion barrier layer) are stacked one on top of another. The lowest interconnect level is that interconnect level closest to the substrate and the highest interconnect level is that furthest away from the substrate.

[0030] Prior to the present invention, wires like dual damascene wire 175A could only be electrically connected to a wiring structure in an adjacent lower interconnect level through a via (for example dual damascene via 180A) and wires like dual damascene wires 175A and 175B could only be electrically connected to a wiring structure in an adjacent upper interconnect level through a via (for example dual damascene via 180A) located in the upper interconnect level. Via bars like dual damascene via bar 180C and 180E allow electrical connection of wiring structures in interconnect level separated by an intervening interconnect level containing the dual damascene via bar.

[0031] Wires carry signals or power horizontally within an interconnect level. Vias carry signals and power vertically

within and between interconnect levels. Via bars carry signals or power both horizontally and vertically within an interconnect level.

[0032] FIG. 3A is a top view and FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A illustrating various combinations of dual damascene wires and dual damascene via bars according to the present invention. In FIGs. 3A and 3B, a lower interconnect level 200 including a dielectric diffusion barrier layer 205 and an ILD layer 210 is formed on top of substrate 105. An upper interconnect level 215 including a dielectric diffusion barrier layer 218 and an ILD layer 220 is formed on top of first interconnect level 200. Dual damascene wires 222, 224, 230 and 272, dual damascene via bars 226, 232, 238, 240, 244, 250, 254, 256, 260 and 268 and dual damascene via 274 are formed in upper interconnect level 215. Dual damascene wires 228, 234, 242, 246, 258, 262 and 276 and dual damascene via bars 236, 248, 252, 262 and 270 are formed in lower interconnect level 200.

[0033] Dual damascene wire 224 is electrically connected to dual damascene wire 228 through dual damascene via bar 226. Dual damascene wire 230 is electrically connected to dual damascene wire 234 through dual damascene via bar 232

and dual damascene wire 234 is further connected to devices in substrate 105 or still lower interconnect levels in substrate 105 through dual damascene via bar 236.

[0034] Dual damascene via bar 240 is electrically to dual damascene wire 242. Dual damascene via bar 244 is electrically connected to dual damascene wire 246 and dual damascene wire 246 is further connected to devices in substrate 105 or still lower interconnect levels in substrate 105 through dual damascene via bar 248. Dual damascene via bar 250 is electrically connected to dual damascene via bar 252 and dual damascene via bar 252 is further connected to devices in substrate 105 or still lower interconnect levels in substrate 105.

[0035] Dual damascene via bar 256 runs over dual damascene wire 258, but is not electrically connected to dual damascene wire 258 because of dielectric diffusion barrier layer 218 intervening between the dual damascene via bar and the dual damascene wire. Dual damascene via bar 260 runs over dual damascene wire 262, but is not electrically connected to dual damascene wire 262 because of dielectric diffusion barrier layer 218 intervening between the dual damascene via bar and the dual damascene wire. Dual damascene wire 262 is further connected to devices

in substrate 105 or still lower interconnect levels in substrate 105 through dual damascene via bar 264. Dual damascene via bar 268 runs over dual damascene via bar 270, but is not electrically connected to dual damascene via bar 270 because of dielectric diffusion barrier layer 218 intervening between the two dual damascene via bars. Dual damascene via bar 270 is further connected to devices in substrate 105 or still lower interconnect levels in substrate 105. It is possible to stack dual damascene via bars that each do not extend through corresponding dielectric diffusion barrier layers of their respective interconnect levels.

[0036] Dual damascene wire 272 is electrically connected to dual damascene wire 276 through dual damascene via 274.

[0037] Dual damascene wires 222, 224 and 230 and dual damascene via bars 238, 240, 244, 250, 254, 256, 260 and 268 may be electrically connected to additional wiring structures (including terminal pads) in an upper and adjacent interconnect level 280 using any of the connection combinations shown between wiring structures in upper and lower interconnect levels 200 and 215. Any number of interconnect levels may so be built up.

[0038] FIG. 4A is a plan view and FIG. 4B is a cross-sectional view

through line 4B-4B of FIG. 4A illustrating an inductor according to the present invention. In FIG. 4A, an inductor 300 includes a stack 305 of spiral shaped conductive dual damascene via bars (see FIG. 4B). A first end 310 of stack 305 is connected to a dual damascene wire 315 by a dual damascene via 320. A second end 325 of stack 305 is connected to a dual damascene wire 330 by a dual damascene via 335.

[0039] Turning to FIG. 4B, a first interconnect level 340 is formed on top of a substrate 345. A second interconnect level 350 is formed on top of first interconnect level 340. A third interconnect level 355 is formed on top of second interconnect level 350. A fourth interconnect level 360 is formed on top of third interconnect level 355. A first spiral shaped conductive dual damascene via bar 365 is formed in first interconnect level 340. A second spiral shaped conductive dual damascene via bar 370 is formed in second interconnect level 350. A third spiral shaped conductive dual damascene via bar 375 is formed in third interconnect level 355. Dual damascene via bar 375 contacts and is electrically connected along the entire length of a bottom surface 380A of dual damascene via bar 375 to the entire length of a top surface 380B of dual dama-

scene via bar 370. Dual damascene via bar 370 contacts and is electrically and connected along the entire length of a bottom surface 385A of dual damascene via bar 370 to the entire length of a top surface 385B of dual damascene via bar 365. While three spiral dual damascene via bars are illustrated in FIG. 4B, any number of spiral via bars in adjacent interconnect levels may be stacked to form an inductor.

[0040] While dual damascene vias 320 and dual damascene via bars 365, 370 and 375 are illustrated in FIG. 4B as having cross-sections that are narrower than, for example dual damascene wire 315, dual damascene via bars 365, 370 and 375 may be as wide as dual damascene wire 315 (with spacing adjustment to leave dielectric material between the coils of inductor 300.

[0041] FIG. 5A is a plan view and FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A illustrating a capacitor according to the present invention. In FIG. 5A, a capacitor 400 includes plates 405A, 405B, 405C, 405D and 405E (see also FIG. 5B). A first end 410B of plate 405B is connected to a dual damascene wire 415 by a dual damascene via 420B. A first end 410D of plate 405D is connected to dual damascene wire 415 by a dual damascene

via 420D. A first end 425A of plate 405A is connected to a dual damascene wire 440 by a dual damascene via 445A. A first end 425C of plate 405C is connected to dual damascene wire 440 by a dual damascene via 445C. A first end 425E of plate 405E is connected to dual damascene wire 440 by a dual damascene via 445E.

[0042] Turning to FIG. 5B, a first interconnect level 440 is formed on top of a substrate 445. A second interconnect level 450 is formed on top of first interconnect level 440. A third interconnect level 455 is formed on top of second interconnect level 450. A fourth interconnect level 460 is formed on top of third interconnect level 455. Each plate 405A, 405B, 405C, 405D and 405E includes a dual damascene via bar 465 formed in first interconnect level 450, a dual damascene via bar 470 formed in second interconnect level 450 and a dual damascene via bar 475 formed in third interconnect level 355. Within each plate 405A, 405B 405C, 405D and 405E, corresponding dual damascene via bars 475 contact and are electrically connected along the entire length of a bottom surface 480A of dual damascene via bar 475 to the entire length of a top surface 480B of each dual damascene via bar 470. Within each plate 405A, 405B 405C, 405D and 405E, corre-

sponding dual damascene via bars 470 contact and are electrically connected along the entire length of a bottom surface 485A of dual damascene via bar 470 to the entire length of a top surface 485B of each dual damascene via bar 465. Dual damascene via bars 475 in different plates 405A, 405B, 405C, 405D and 405E do not contact and are not electrically connected to each other. Dual damascene via bars 470 in different plates 405A, 405B, 405C, 405D and 405E do not contact and are not electrically connected to each other. Dual damascene via bars 465 in different plates 405A, 405B, 405C, 405D and 405E do not contact and are not electrically connected to each other. While three levels of dual damascene via bars are illustrated in FIG. 4B, any number of interconnect levels containing via bars may be stacked to form plates of a capacitor.

[0043] Thus the present invention provides new wiring structures that improve dual damascene wire fabrication and dual damascene wiring efficiency.

[0044] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein,

but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.